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In the Claims:

1. (Currently Amended) A clock filter for an electronic device, the clock filter comprising:

a clock receiver electrically coupled to an external clock; and

an enabling circuit electrically coupled to the clock receiver;

wherein the clock receiver generates an internal clock signal and the enabling circuit disables the clock receiver for a first time period after ~~detecting~~ being triggered by a transition on the internal clock signal.

2. (Original) The clock filter of claim 1, wherein the enabling circuit includes a pulse generator.

3. (Original) The clock filter of claim 2, wherein the pulse generator is electrically coupled to the clock receiver, and the pulse generator generates a pulse signal having a duration substantially equivalent to the first time period.

4. (Original) The clock filter of claim 3, wherein the clock receiver is disabled when the pulse signal is high.

5. (Original) The clock filter of claim 1, wherein the enabling circuit is electrically coupled to a clock filter enable signal.

6. (Original) The clock filter of claim 5, wherein the enabling circuit disables the clock receiver when the clock filter enable signal is enabled.

7. (Currently Amended) A clock filter for an electronic device, the clock filter comprising:

a clock receiver electrically coupled to an external clock signal, the clock receiver generating an internal clock signal;

a pulse generator electrically coupled to the clock receiver, the pulse generator generating a pulse signal for a first time period upon ~~detecting~~ being triggered by a transition in the internal clock signal; and

an enabling circuit electrically coupled to the pulse generator and the clock receiver, the enabling circuit being electrically coupled to a clock filter enable signal and disabling the clock receiver for a duration of the first time period when the clock filter enable signal is enabled.

8. (Original) The clock filter of claim 7, wherein the enabling circuit is electrically coupled to a clock enable signal, the enabling circuit disabling the clock receiver when the clock enable signal is reset.

9. (Original) The clock filter of claim 7, wherein the enabling circuit includes:

a NAND gate electrically coupled to the pulse generator and the clock filter enable signal; and

an AND gate electrically coupled to the NAND gate such that the output of the NAND gate is a first input to the AND gate.

10. (Original) The clock filter of claim 9, wherein the AND gate has a second input electrically coupled to a clock enable signal.

11. (Original) The clock filter of claim 9, wherein an output of the AND gate is electrically coupled to the clock receiver.

12. (Previously Presented) The clock filter of claim 7, wherein the enabling circuit includes:

a first NAND gate electrically coupled to the pulse generator and the clock filter enable signal;

a second NAND gate electrically coupled to an output of the first NAND gate; and

an inverter electrically coupled to an output of the second NAND gate, wherein the output of the inverter is electrically coupled to the clock receiver.

13. (Original) The clock filter of claim 12, wherein the second NAND gate has a second input electrically coupled to a clock enable signal.

14. (Original) The clock filter of claim 12, wherein the first NAND gate has a second input electrically coupled to a test mode enable signal.

15. (Original) The clock filter of claim 7, wherein the first time period is about 5% to about 10% of a transition period of the external clock signal.

16-21. (Canceled)

22. (Previously Presented) A clock filter for an electronic device, the clock filter comprising:

a clock receiver electrically coupled to an external clock signal and a clock receiver enable signal, the clock receiver generating an internal clock signal having a first pulse of a first duration;

a pulse generator electrically coupled to the clock receiver to receive the internal clock signal, the pulse generator generating a second pulse signal for a second duration upon detecting a transition in the internal clock signal, the second duration being less than the first duration; and

an enabling circuit electrically coupled to the pulse generator to receive the second pulse and electrically coupled to the clock receiver to provide the clock receiver enable signal, the enabling circuit further electrically coupled to a clock enable signal, the enabling circuit disabling the clock receiver via the clock receiver enable signal during the second duration if the clock enable signal is enabled.

23. (Previously Presented) The clock filter of claim 22, wherein the enabling circuit includes:

a NAND gate electrically coupled to the pulse generator, the NAND gate receiving a clock filter enable signal and the second pulse as input; and

an AND gate electrically coupled to the NAND gate such that an output of the NAND gate is a first input to the AND gate and a second input to the AND gate is the clock enable signal and an output of the AND gate is the clock receiver enable signal.

24. (Previously Presented) The clock filter of claim 22, wherein the enabling circuit includes:

a first NAND gate electrically coupled to the pulse generator, the first NAND gate receiving a clock filter enable signal and the second pulse as input;

a second NAND gate electrically coupled to the first NAND gate, the second NAND gate receiving an output of the first NAND gate and the clock enable signal as input; and

an inverter electrically coupled to the second NAND gate, the inverter receiving an output of the second NAND gate as input and providing the clock receiver enable signal as output.

25. (Previously Presented) The clock filter of claim 22, wherein the second duration is about 5% to about 10% of the first duration.

26. (Previously Presented) The clock filter of claim 22, wherein the clock receiver maintains the internal clock signal as a substantially constant level when the clock receiver enable signal is disabled.